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Ambipolar field-effect transistors by few-layer InSe with asymmetry contact metals

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Group IIIA–VIA layered semiconductors (MX, where M = Ga and In, X = S, Se, and Te) have attracted tremendous interest for their anisotropic optical, electronic, and mechanical properties. In this study, we demonstrated that metal and InSe junctions can lead to carrier behaviors in few-layered InSe FETs. These results indicate that the polarity of few-layered InSe FETs can be determined by using metals with different work functions. We adopted FET S/D metal contacts with asymmetric work functions to reduce the Schottky barriers of electrons and holes, and discovered that few-layered InSe FETs with carefully selected metal contacts can achieve ambipolar behaviors. These results indicate that group IIIA–VIA layered semiconductor FETs with asymmetry contact metals have great potential for applications in photovoltaic devices, optical sensors, and CMOS inverter circuits. [http://dx.doi.org/10.1063/1.4995589]

Graphene was the first two-dimensional (2-D) material to be discovered. It shows high carrier mobility, with theoretical values of 10^6 cm^2 V^{-1} s^{-1} at 2 K[1] and 15,000 cm^2 V^{-1} s^{-1} at room temperature,[2] although it lacks a bandgap. By contrast, 2-D transition metal dichalcogenides show sizable bandgaps with chalcogenide atoms in two hexagonal planes separated by a plane of metal atoms, suiting them to applications in electrical and optoelectronic devices such as transistors, solar cells, photodetectors, and electroluminescent devices. In optoelectronic devices, the injection of electrons and holes has a considerable impact on performance. Some research groups have used separate gates at the drain and source sides to study the use of 2-D materials in optoelectronics applications.[3] This dual-gate structure enables more efficient hole and electron injection in Tungsten Diselenide (WSe_2) FETs.[3] Moreover, WSe_2 bulk materials, which have an indirect bandgap, become direct bandgap semiconductors when being reduced to a single layer,[4,5] indicating that their energy bandgaps are very sensitive to the layer thickness. The monolayer of WSe_2 is not easy to be fabricated. In contrast, indium selenide (InSe) is a group IIIA–VIA layered semiconductor (MX, where M = Ga and In and X = S, Se, and Te). Compared to monolayered InSe, few-layered InSe has a direct bandgap and it is relatively easier to be fabricated. In addition, few-layered InSe has gained renewed interest for its anisotropic optical, electronic, and mechanical properties and has applications in memory devices, optical sensors, and thermoelectric implements.[6] The influence of InSe and metal's Schottky barrier on the injection of carriers is one of the most important factors of fabricating highly efficient optoelectronic devices; therefore, the junction of metal/InSe is one of the most urgent issues that need to be addressed.

In this work, we adopted few-layered InSe,[7,8] which is a direct bandgap material, to fabricate ambipolar FETs through work function engineering. We controlled the Schottky barrier of holes and electrons by using metals with different work functions as contacts to study the characteristics of

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few-layered InSe ambipolar behaviors, which lend group IIIA–VIA layered semiconductors great potential for applications in photovoltaic devices, optical sensors, and CMOS inverter circuits.

A structure containing single-gate electrodes with different metals as source and drain contacts was fabricated in this study. Fig. 1 illustrates the device structure of the ambipolar FET and side views of the hexagonal structure of InSe crystal. InSe is a layered crystal arranged in a hexagonal lattice consisting of four close-packed monatomic sheets in the sequence Se–In–In–Se, and therefore can be mechanically exfoliated using the Scotch tape method.

The synthesized single-crystal InSe flakes were exfoliated into few-layered InSe nanosheets by using a Scotch tape mechanical exfoliation process. The bulk InSe crystal was placed on an adhesive tape, and the few-layered InSe layers were peeled off by rubbing and slicing the tape for several times. The peeled layers in the scotch tape were first transferred to the Polydimethylsiloxane (PDMS) and then to the aluminum oxide (Al_2O_3)-coated $p^{++}Si$ wafer, as shown in figure 2. A few-layered InSe FET with Al and Pd as the source and drain contacts, respectively, was fabricated. First, the shadow mask was aligned on the exfoliated few-layered InSe nanosheets. Subsequently, 70-nm-thick layers of Al and Pd were deposited by an evaporator. Then, the transferred few-layered InSe nanosheets were inspected using an optical microscope. The thickness of the as-fabricated few-layered InSe

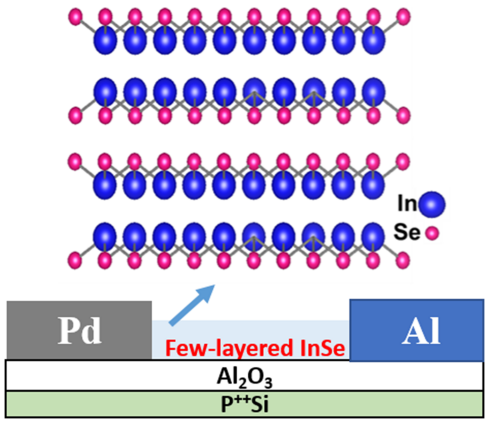

FIG. 1. Device structure of the ambipolar FET studied in this work and side view of the hexagonal structure of InSe crystal.

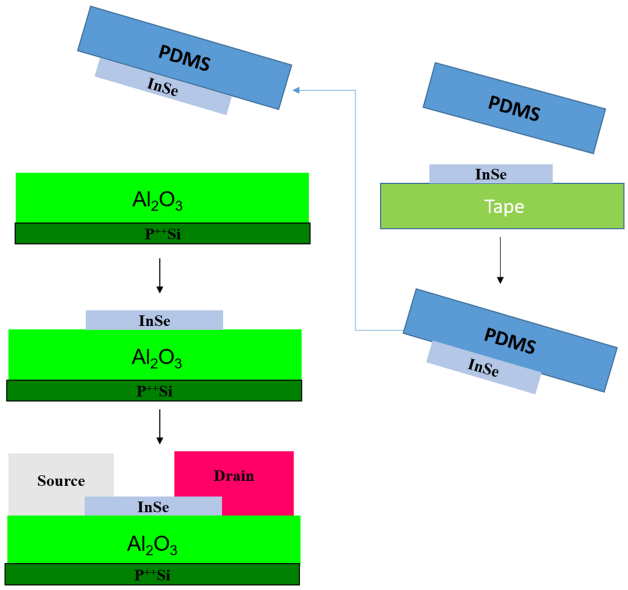

FIG. 2. The fabrication processes for the ambipolar FETs.

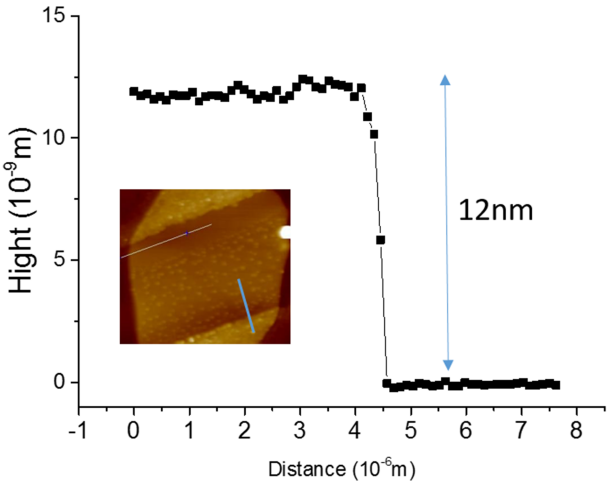

FIG. 3. AFM image of InSe channel region. The thickness of few-layered InSe is 12 nm, corresponding to 14 layers of InSe.

was determined by atomic force microscopy (AFM), as illustrated by figure 3. The thickness of few-layered InSe is 12 nm, corresponding to 14 layers of InSe.

Fig. 4 shows three schematic structures for 2-D FETs with different metals as contacts. On device I, 70-nm Pd layers were deposited as source and drain contact electrodes; on device II, we used 70-nm layers of Al; and on device III, we used a 70-nm layer of Al and a 70-nm layer of Pd as the source and drain contact electrodes, respectively. We also used a 30-nm layer of Al_2O_3 as a gate insulator to reduce the control voltage and study the influence of the contact metal on all of the devices. The energy levels of the materials used in this work are shown in Fig. 4. The conduction band (CB) and valance band (VB) energy levels of InSe are 4.3 eV and 5.6 eV, respectively. The work function of Pd is 5.4 eV, which can enhance the injection of holes into the valance band of InSe. The work function of Al is 4.2 eV, which can enhance the injection of electrons into conduction band. We adopted FET S/D metal contacts with asymmetric work functions to reduce the Schottky barriers of electrons and holes to study ambipolar behavior.

The transfer curves of device I and device II and the corresponding energy band bending of the InSe FETs are shown in Figure 5(a). The blue line and the black line show typical p-type and n-type FET behavior, respectively. The linear mobility was extracted from the linear-regime

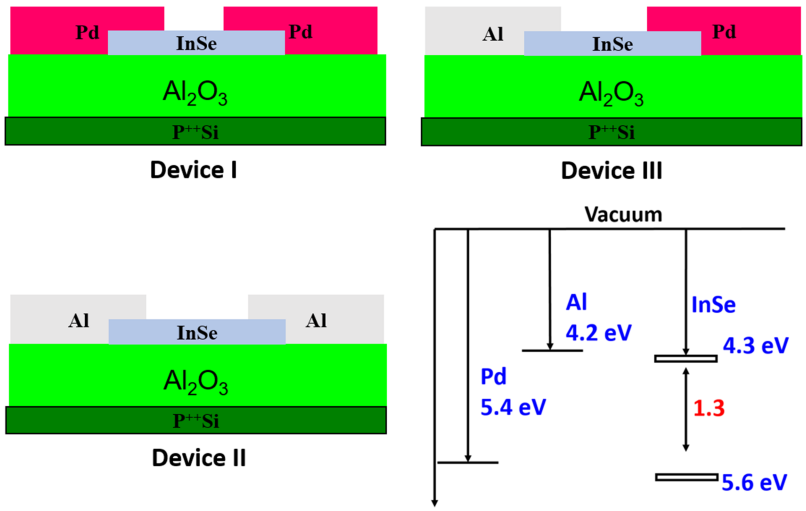

FIG. 4. Three schematic structures of 2-D FETs with different metals as contacts. The lower right figure shows the energy levels of the materials used: Pd, Al, and InSe.

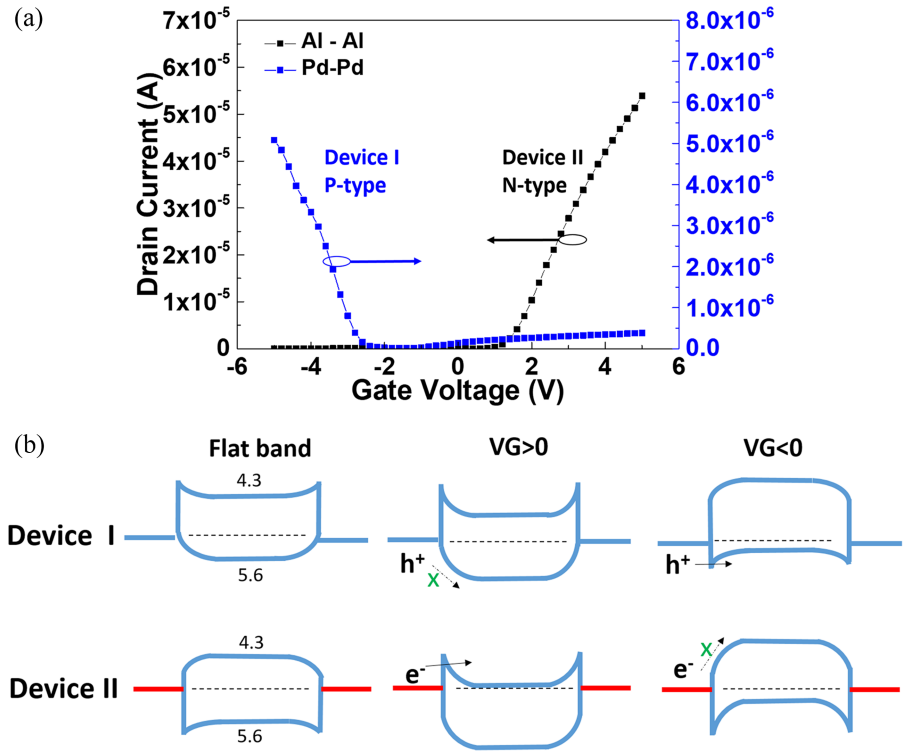

FIG. 5. (a) The transfer curve of Pd-Pd and Al-Al InSe FETs, and corresponding energy band bending of InSe FETs. (b) Transfer curves of Pd-Pd and Al-Al InSe FETs, and corresponding energy band bending.

transconductance gm at the low drain-to-source voltage (V_{DS} = 1V) by,[9]

$$\mu_{lin} = \frac{L g_m}{W C_i V_{DS}}$$

where C_i denotes the capacitance of the gate insulator per unit area, and L and W are the channel length and channel width, respectively. gm is the transconductance defined by,

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=1V}$$

where I_D and V_{GS} denote the drain current and the gate voltage, respectively. The threshold voltage (V_{th}) was determined by plotting $I_D^{1/2}$ versus V_{GS} and extrapolation the curve to zero drain current.[10] The on/off ratio was estimated from the transfer characteristics at V_{DS} = 1 V by calculating the ratio between the maximal on current (at V_{GS} = 1 V) and the minimal off current. The channel width and channel length of the TFTs were 6 μm and 12 μm, respectively. From the characteristics of the type-I device, a linear mobility (μ_{lin}) of 39.8 $cm^2/V{\cdot}sec.$, a threshold voltage (V_{th}) of -2.5 V, and an on/off current ratio of 5.8 x 10^2 are extracted. From the characteristics of the type-II device, a linear mobility (μ_{lin}) of 63.2 $cm^2/V{\cdot}sec.$, a threshold voltage (V_{th}) of 0.9 V, and an on/off current ratio of 2.69 x 10^4 are extracted.

These results indicate that the polarity of an InSe FET can be controlled by using metals with different work functions. Furthermore, this phenomenon can be realized by using the energy band bending of the InSe FETs. Device I exhibited a low hole-injection barrier and device II exhibited a low electron-injection barrier, as shown in the inset of figure 5(b). As the figure 5(b) of device I illustrates, in the flat bend energy diagram, Pd work function is 5.4 eV near VB (5.6eV), so when positive gate bias (Vg>0), the band bending increases the Schottky barrier of holes and prohibits the injection of holes into VB. In contrast, when negative gate bias (Vg<0), the band bending reduces the Schottky barrier of holes and enhances the injection of holes into VB. This bending caused device I to show p-type FET transfer curves. Similarly, as the figure 5(b) of device II illustrates, in the flat bend

energy diagram, Al work function is 4.2 eV near CB (4.3 eV), so when positive gate bias (Vg>0), the band bending reduces the Schottky barrier of electrons and enhances the injection of electrons into CB. In contrast, when negative gate bias (Vg<0), the band bending increases the Schottky barrier of electrons and prohibits the injection of electrons into CB. This bending caused device II to show n-type FET transfer curves. This method was successful for revealing the characteristics of few-layered InSe ambipolar behavior.

The transfer curve of device III and the corresponding energy band bending of the InSe FET are shown in Fig. 6(a). As illustrated in the left band diagram of Fig. 6(a), the holes can easily be injected into the valence band by negative gate bias and form a p-channel. From the characteristics of the type-III device, a p-type linear mobility (μ_{lin}) of 6.6 $cm^2/V{\cdot}sec.$, a threshold voltage (V_{th}) of -1 V, and an on/off current ratio of 1.1 x 10^2 are extracted. As the right band diagram of Fig. 6(a) shows, electrons can easily be injected into the conduction band by positive gate bias and form an n-channel. From the characteristics of the type-III device, an n-type linear mobility (μ_{lin}) of 57.9 $cm^2/V{\cdot}sec.$, a threshold voltage (V_{th}) of 0.5 V, and an on/off current ratio of 3.7 x 10^2 are extracted.

The transfer curve of device III shows clear ambipolar behavior. Fig. 6(b) shows the output curve of device III, which has a linear region similar to that of device I. The higher Vd reduced the depth of the n-channel on the drain side, but the p-channel was induced when Vd > Vg. The drain current rises again with the drain voltage because the p-channel is formed when a larger Vd is applied. Given the output curve of device III, we can infer that hole injection and electron injection occur simultaneously.

We conducted a series of experiments to demonstrate that metal and InSe junctions can lead carrier behavior of FETs. These results indicate the polarity of few-layered InSe FET can be determined by using different metal work functions. We adopted FET S/D metal contacts with asymmetric work functions to reduce the Schottky barriers of electrons and holes. This study is the first one that finds few-layered InSe FETs with carefully selected metal contacts can achieve ambipolar behaviors. These results make group IIIA−VIA layered semiconductors have great potential in

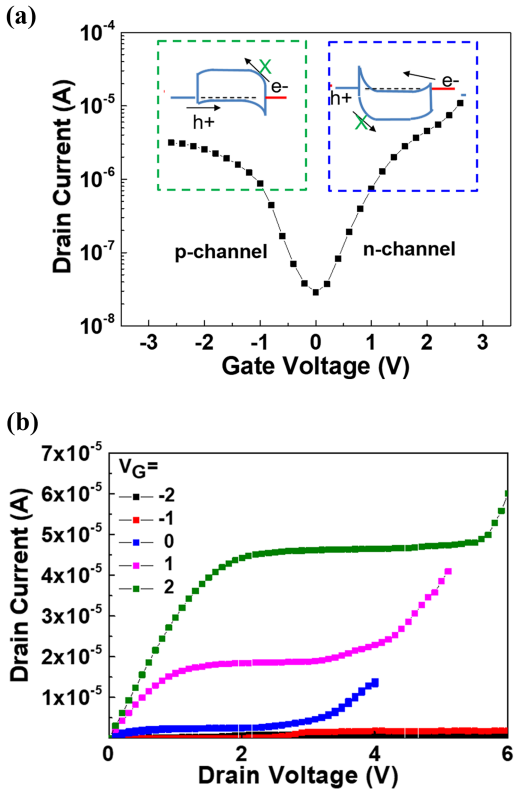

FIG. 6. Electrical characteristics of device III: (a) transfer curve; (b) output curve.

photovoltaic devices, light-emitting devices, photodetectors, anisotropic-optoelectronic device, and CMOS inverter circuits.

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