A Bi-Anti-Ambipolar Field Effect Transistor

Christy Roshini Paul Inbaraj, Roshan Jesus Mathew, Rajesh Kumar Ulaganathan, Raman Sankar, Monika Kataria, Hsia Yu Lin, Yit-Tsong Chen, Mario Hofmann,* Chih-Hao Lee, and Yang-Fang Chen*

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Multistate logic is recognized as a promising approach to increase the device density of microelectronics, but current approaches are offset by limited performance and large circuit complexity. We here demonstrate a route toward increased integration density that is enabled by a mechanically tunable device concept. Bi-anti-ambipolar transistors (bi-AATs) exhibit two distinct peaks in their transconductance and can be realized by a single 2D-material heterojunction-based solid-state device. Dynamic deformation of the device reveals the co-occurrence of two conduction pathways to be the origin of this previously unobserved behavior. Initially, carrier conduction proceeds through the junction edge, but illumination and application of strain can increase the recombination rate in the junction sufficiently to support an alternative carrier conduction path through the junction area. Optical characterization reveals a tunable emission pattern and increased optoelectronic responsivity that corroborates our model. Strain control permits the optimization of the conduction efficiency through both pathways and can be employed in quaternary inverters for future multilogic applications.
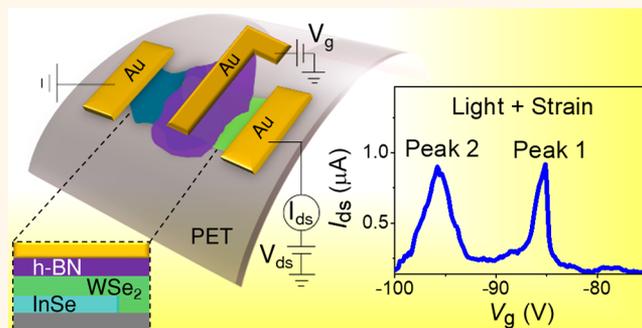
The continued scaling of device density in microelectronics is a focus of significant research efforts due to the societal impact of computers and integrated circuits. One major challenge is the achievable integration density of interconnects since their number density in connected networks generally increases faster than the transistor number.[1,2] To solve this issue, multilevel logic has been suggested as a route for increasing the information density per interconnect.[2] The limited proliferation of multilevel logic in the last four decades is due to several challenges that arise from shortcomings of current device realizations. Multistable operation at several voltage levels, the foundation of multiple logics, requires nonmonotonic current−voltage behaviors, which have mainly been realized using the negative differential resistance (NDR) region of resonant-tunneling diodes.[3] However, this approach produces large amounts of dissipated static power, limiting the efficiency of the circuit. Moreover, the gained information density of multilevel logic is offset by the increasing complexity of suitable device architectures.[4] Finally, complex fabrication techniques are required to realize devices with distinct and well-adjusted current−voltage characteristics.[4−6]

We here demonstrate an approach to realizing quaternary logic in a single 2D materials heterojunction device termed "bi-anti-ambipolar transistor" (bi-AAT). Quaternary logic, i.e., the

implementation of four distinct logic levels, is particularly suitable for hybrid multilogic/digital electronics[2,7] and is enabled by a mechano-optically adjustable operating mechanism of our bi-AAT. Upon gating a 2D InSe/WSe₂ heterojunction device, negative differential transconductance can be observed, which shows significantly higher peak-voltage ratios than NDR devices, promising higher power efficiencies. Unlike conventional anti-ambipolar transconduction (AAT) devices, our device exhibits two distinct peaks in the transconductance curve.

Characterization of the bi-AAT device under dynamic deformation reveals that the observed dual-peak structure in the transconductance originates from the competition of two distinct carrier pathways through the heterojunction device. Under unstrained conditions, carrier conduction is controlled by the edge of the junction due to current bunching. However, upon illumination and application of strain, the junction conductance increases sufficiently to support a second
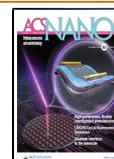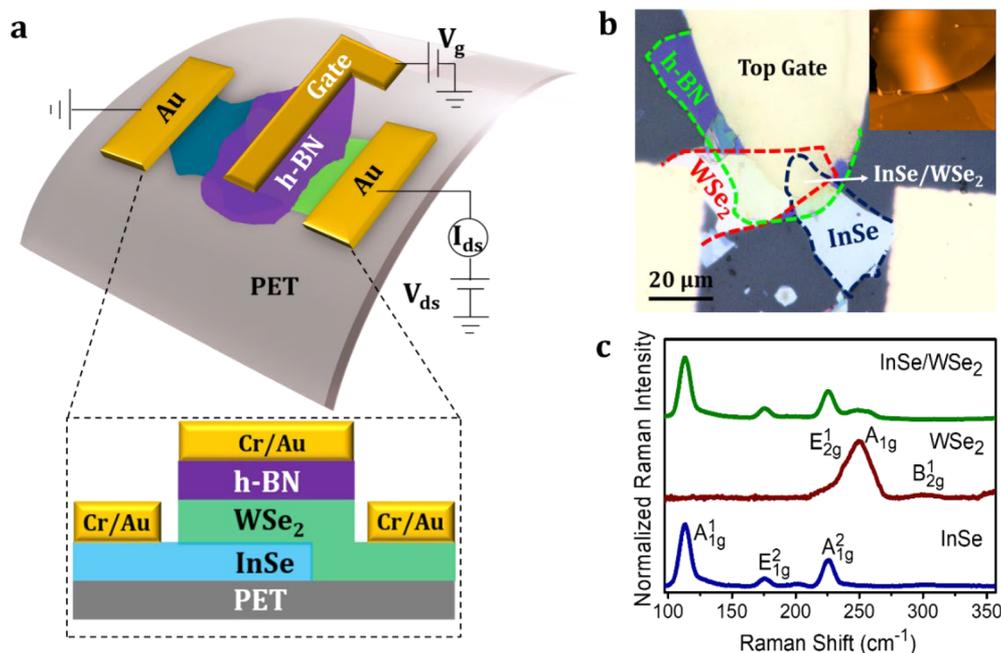
Figure 1. Device structure on a flexible PET substrate. (a) Schematic illustration of the InSe/WSe$_2$ heterostructure device along with the electrode connection. (b) Optical microscope image of the assembled heterostructure with the inset showing the AFM image of the same. (c) Raman spectra of the InSe, WSe$_2$, and InSe/WSe$_2$ region in the stacked heterostructure.

conduction pathway through the face of the junction. The strain-enhanced recombination in the junction furthermore leads to hybrid photoemission peaks and changes the optical responsivity of the InSe/WSe$_2$ heterostructure. Optimizing the relative contribution of the conduction pathways yields two transconductance peaks with similar height and good separation. The potential of bi-AAT devices is demonstrated in the form of a quaternary inverter from a single solid-state device, thus reducing the complexity and increasing the integration density of multilevel logic devices for future electronics.

RESULTS AND DISCUSSION

Our bi-AAT device is based on a heterojunction between a few-layered InSe, WSe$_2$, and h-BN that were obtained by a mechanical exfoliation technique from bulk crystals (more details on the single-crystal growth procedures and crystal structures can be found in Supplementary Notes 1 and 2, respectively). The semiconducting 2D material constituents were chosen due to the complementary electronic structure of InSe and WSe$_2$, which depends on the number of layers[8−10] and results in a heterojunction with type-II band alignment. We employed multilayers of these materials because of their high and comparable intrinsic carrier mobility (InSe, $\mu_e \approx 10^3$ cm^2/(V s); WSe$_2$, $\mu_h \approx 10^2$ cm^2/(V s)),[11−13] resulting in similar transconductance values. These 2D materials junctions were produced on flexible polyethylene terephthalate (PET) substrates using established dry transfer techniques using polydimethylsiloxane (PDMS) stamping,[14,15] and a detailed schematic of each step is shown in Figure S3. Finally, h-BN top gates were deposited to selectively gate the junction area. The resulting device structure is illustrated in Figure 1a, and the optical microscopy image and atomic force microscopy (AFM) image of the fabricated device are presented in Figure 1b. The investigated device contained InSe and WSe$_2$ flakes with thicknesses of ∼17 nm and ∼14 nm, respectively (Figure S4).

The vibrational modes of the individual InSe, WSe$_2$ region, and InSe/WSe$_2$ heterojunction were confirmed by Raman spectroscopy, as shown in Figure 1c. The InSe region shows strong vibrational peaks at 115, 178, and 228 cm^{-1}, corresponding to out-of-plane A$^1_{1g}$, in-plane E$^2_{1g}$, and out-of-plane A$^2_{1g}$ modes, as reported previously.[15,16] The WSe$_2$ region exhibits a broad peak at 250 cm^{-1}, a combination of E$^1_{2g}$ and A$_{1g}$ modes, and the characteristic of the few-layered WSe$_2$, and the small peak at 302 cm^{-1} corresponds to the B$^1_{2g}$ mode.[17] The overlapped InSe/WSe$_2$ region exhibits all the prominent peaks of InSe and WSe$_2$, but the intensity is quenched due to interlayer coupling.

The transfer characteristics of the individual InSe and WSe$_2$ flakes are obtained by sweeping gate voltage (V_g) at a constant drain−source voltage (V_{ds}) and presented in Figure 2a and b, respectively. It can be seen that InSe exhibits n-type behavior, while WSe$_2$ shows p-type conduction. The transfer curve for the InSe/WSe$_2$ heterojunction device is shown in Figure 2c. Anti-ambipolar device characteristics are confirmed by a peak in transconductance between $V_g = -25$ and -5 V. At $V_{ds} = 5$ V, the gate voltage for the maximum conductance (V_{peak}) occurs at ∼−14 V, and the peak to valley ratio (PVR), defined as the ratio between the maximum and the minimum drain−source current (I_{ds}), is ∼10^4 (Figure S5), comparable to the previously reported anti-ambipolar transistors.[18−21] The on-state V_g for the heterojunction transistor ranges between −25 and −5 V ($\Delta V_g \approx 20$ V).

An important observation is the dependence of the p-channel threshold voltage (V_{th}) and peak current (I_{peak}) on the applied bias (Figure 2d). To explain this effect, we conduct simulations (see Supplementary Note 6) of the voltage distribution at gate voltages above the p-channel threshold voltage (Figure 2e).[22] In this condition, the voltage can be seen to drop mainly across the p-channel, resulting in a pinch-off condition at V_{th} for flow through the heterojunction. A more positive drain voltage will modify the pinch-off condition to not occur until a larger negative voltage is applied, in
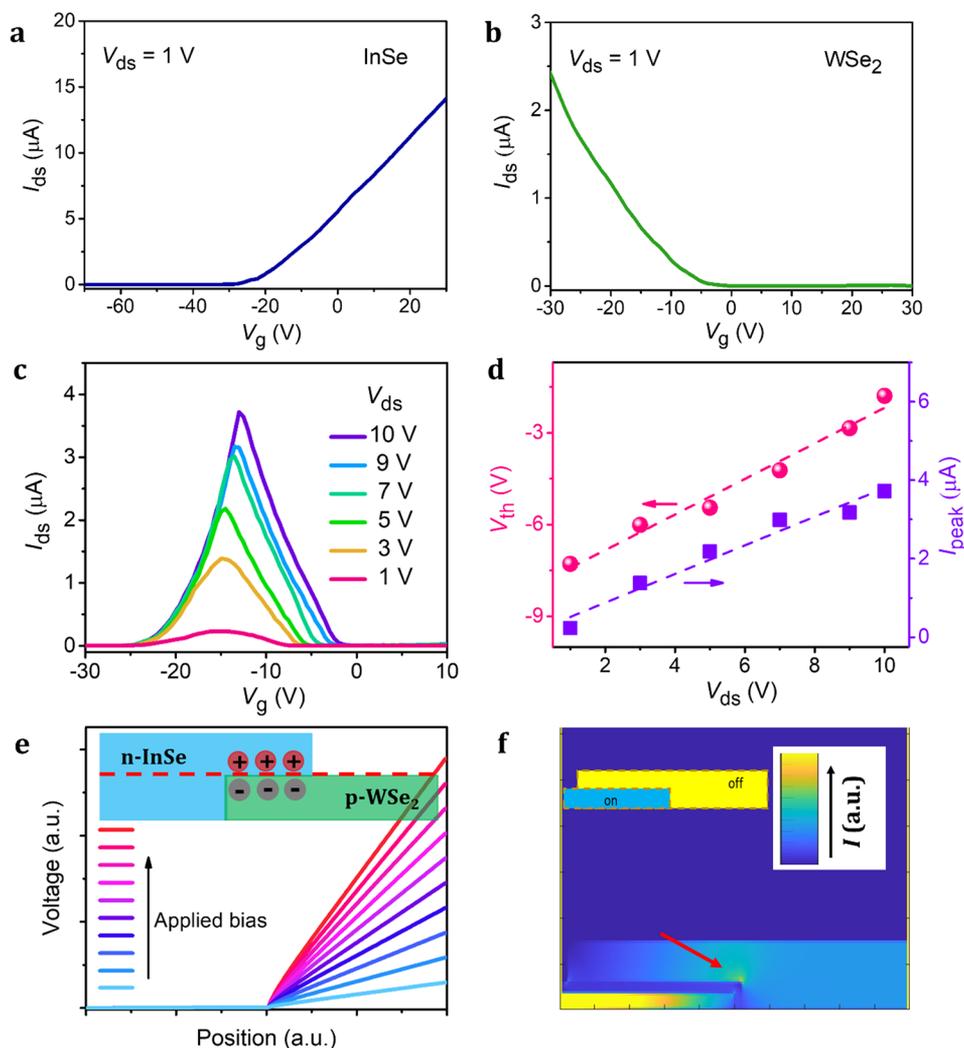
Figure 2. Transfer characteristics of the InSe/WSe$_2$ heterostructure on a solid substrate. (a and b) I_{ds}–V_g curve of the individual InSe and WSe$_2$ devices, respectively. (c) Transfer characteristics of the heterostructure device obtained by sweeping the gate voltage at a constant V_{ds}. (d) Change in threshold voltage (V_{th}) and peak current (I_{peak}) as a function of the applied drain−source voltage. (e) Simulation of the voltage distribution at a cut across the heterojunction as indicated in the inset. (f) Simulation of the spatial current distribution showing current bunching along the leading edge of the heterojunction.

agreement with our observation. The different conductivities of the p and n channels can also explain previous results that highlighted the importance of edge injection.[23] Our simulation of the current flow indicates current bunching at the leading edge (Figure 2f). This effect occurs because injection through the junction face would require carriers to traverse longer regions of the switched-off p-channel.

To prove this hypothesis of simultaneous carrier transport through vertical and lateral (edge) injection, we dynamically modify the conduction pathway by applying mechanical strain to the device by bending the whole device on the flexible PET substrate. This deformation introduces a well-defined uniaxial strain on the top surface (Figure 3a) that extends the channel lengths (see Supplementary Note 7). As with the change in bias voltage, a longer p-channel will change the pinch-off voltage toward more negative gate voltages,[23] and we indeed observe a clear change in the threshold voltage with the strain (Figure 3b). A slope of 40 V/% can be extracted, which indicates an off-channel resistance of 2 MΩ/μm, in agreement with the experimental value for the p-type channel.

Interestingly, when applying both strain and laser illumination, the transfer curve exhibits two "ON" states (Figure 3c), and we label this behavior as "bi-AAT". Due to the application of a top-gate that is selectively positioned on the junction area, previously suggested anti-ambipolar injection processes can be ruled out.[24,25] When comparing different amounts of strain, we observe that the peak position of the original AAT peak (peak 1 in Figure 3c) only shifts and does not decrease in peak current, while the second peak (peak 2 in Figure 3c) shifts in threshold voltage and increases in peak current. We furthermore find that the additional AAT peak shifts less (∼20 V/%) with strain than the main peak (∼40 V/%) (Figure S6). Since the peak shift with strain is indicative of the increasing conduction path length between the electrode and current injection point, this observation suggests that the two peaks have different origins and that the second peak corresponds to a conduction path that has a less localized current injection point.

All these observations can be explained when considering a strain and light-induced increase of the junction conductance that separates the p-channel and n-channel. Simulations (see
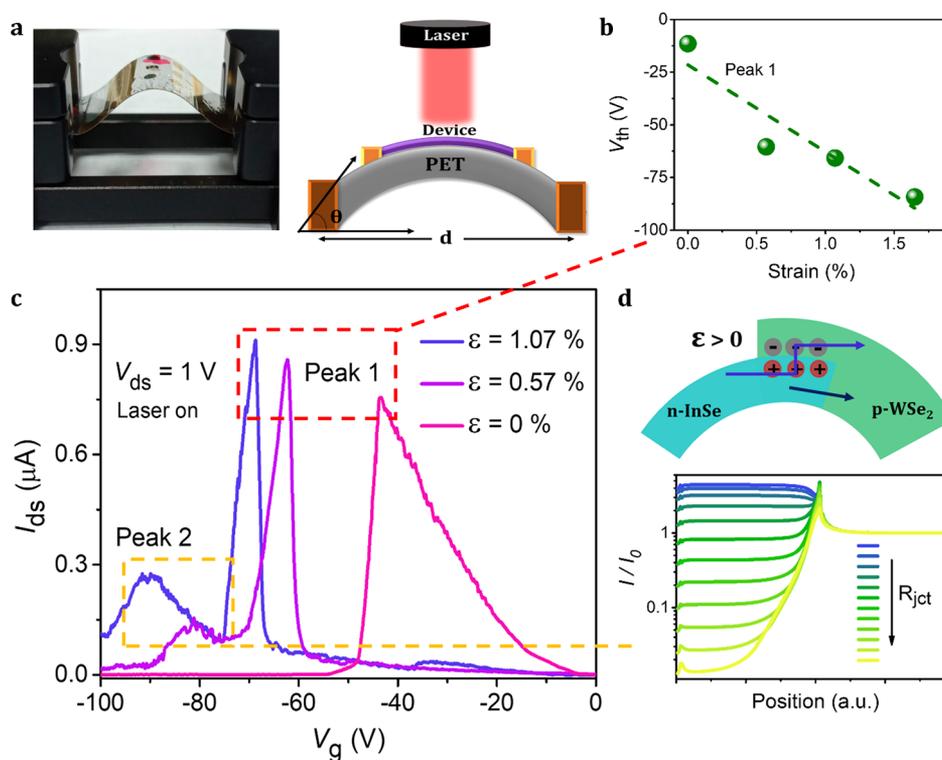
Figure 3. Transfer characteristics of the InSe/WSe$_2$ heterostructure on a flexible PET substrate. (a) Photograph of the custom-made metal clamp setup used for applying strain to the device and schematic representation of the tensile strain application and laser illumination on the device. (b) Change in threshold voltage (V_{th}) of peak 1 as a function of applied strain. (c) Transfer characteristics of the device were measured at different strain conditions with a constant laser power illumination and a constant V_{ds}. (d) Schematic illustration of two parallel conduction pathways taking place in the vertical p−n junction with an increase in strain and the graph showing the current distribution along with the interface for different junction resistance values.

Supplementary Note 6) show that an enhanced junction conductance can increase the current that is being injected through the junction area (Figure 3d). Based on this picture, two conduction pathways are occurring simultaneously in heterojunction devices. Edge injection is usually the dominating mechanism for conduction between the p-channel and n-channel, but if the junction conductivity can be sufficiently lowered, injection through the junction area can occur. The selection of the dominating pathway through external factors can also resolve previous contradicting results on identical AAT devices.[26] In our device, the two competing pathways can be distinguished by their difference in threshold voltages originating from the difference in carrier path length, giving rise to two distinct AAT peaks.

To investigate the origin of the increased junction conductivity upon straining, we conduct spectroscopic characterization (Figure 4a). Photoluminescence measurements at varying amounts of strain show an increase in emission intensity (Figures 4b, S7), corroborating the enhanced recombination in the junction. A closer inspection of the emission spectra at $\varepsilon = 0\%$ shows three peaks that can be assigned to the emission of the constituents (peak A corresponding to InSe,[27,28] peaks B and D corresponding to indirect and direct optical transition in WSe$_2$[29−31]). However, with the application of strain, we observe an additional emission peak that increases with the strain (Figure 4c,d). This peak can be assigned to a hybrid emission peak (peak C in Figure 4b,c) due to an enhanced interlayer recombination[32] (Figure 4d). Photocurrent measurements also demonstrate an enhanced junction conductance. Figure S8a shows the

photoresponse study of the device under dark and 633 nm laser-illuminated conditions at different power densities without strain (in the plane state). The photocurrent increases with an increase in laser power. When the strain is applied ($\varepsilon = 0.57\%$), at a constant laser power, both forward and reverse current increases, as shown in Figure S8b. However, with a further increase in strain ($\varepsilon = 1.07, 1.65\%$), there is no observable change in the forward current, but the reverse current increases systematically with the strain (Figure S8b).

There is a noticeable enhancement in photocurrent ($I_{ph} = I_{light} − I_{dark}$) at $V_{ds} = −5$ V with an increase in strain. The absolute values of photoresponsivity (R) at constant laser power ($P = 7\ \mu$W cm^{-2}) and change in strain are estimated using eq 1 and plotted as a contour plot as represented in Figure 4e.

$$R = \frac{I_{ph}}{P \times A} \tag{1}$$

Here, P is the incident laser power density and A is the active area of the InSe/WSe$_2$ device.[15,28,33] This enhancement of responsivity under reverse bias is due to the added potential created by the application of strain that efficiently separates the photogenerated electron−hole pairs (Figures S9 and 4g). Therefore, we observe a systematic increase in the photoresponsivity as the applied strain increases (reverse bias in Figure 4e,f).

Taking together the results of PL spectra (Figure 4b) and electrical measurement (forward bias condition in Figure 4e,f), it is clear that under the application of external tensile strain interlayer recombination takes place that decreases the
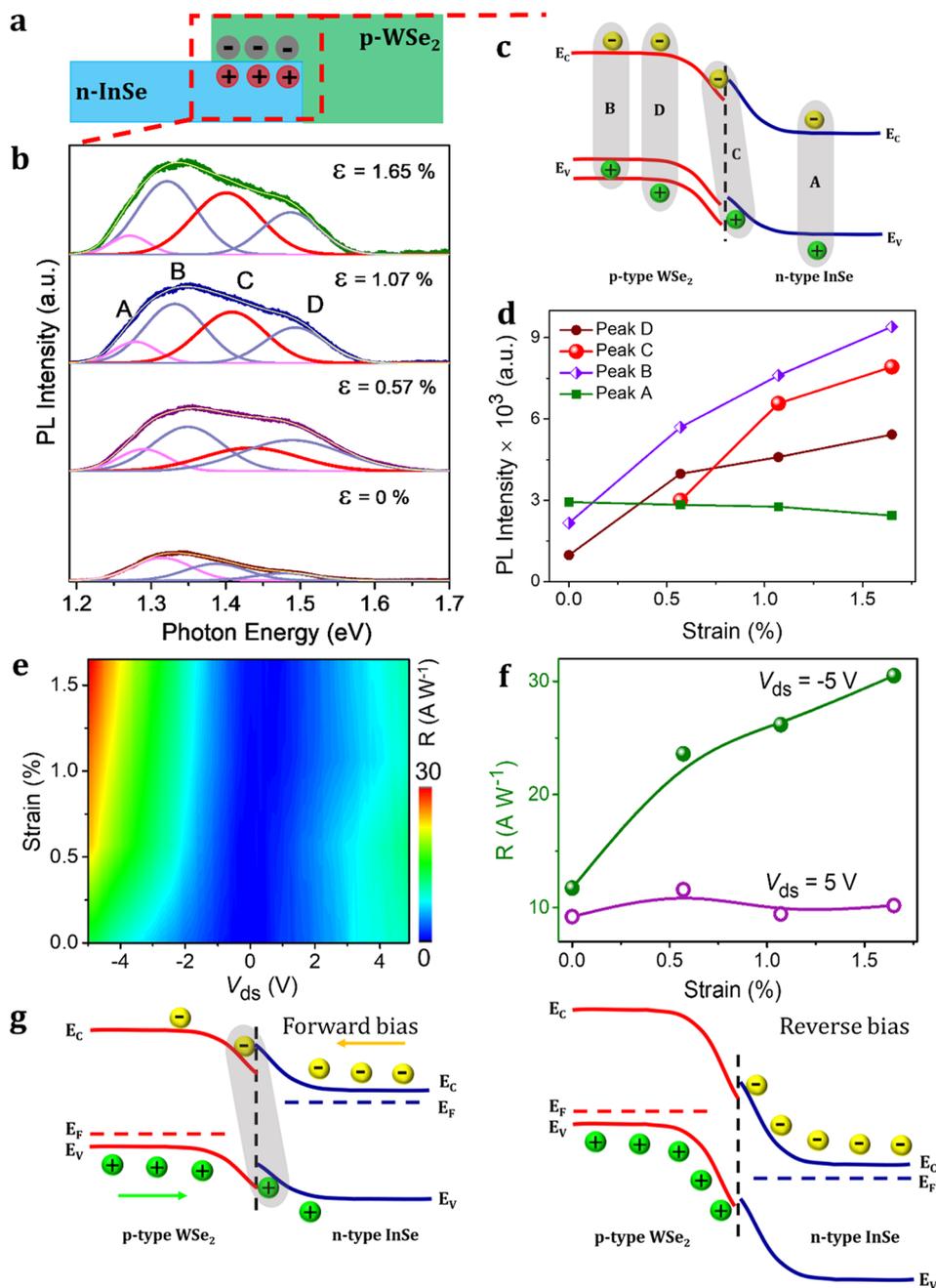
Figure 4. Optoelectronic studies of the InSe/WSe₂ heterostructure. (a) Schematic illustration of the InSe/WSe₂ heterojunction. (b) PL spectra were recorded on the InSe/WSe₂ heterojunction region with and without the application of systematic tensile strain. (c) Energy band diagram representing the optical transitions in the InSe/WSe₂ heterostructure with applied strain. (d) Change in PL peak intensity plotted as a function of strain. (e) Contour plot of the photoresponsivity (R) as a function of applied bias and strain (under 633 nm laser illumination). (f) Photoresponsivity (R) of the device at V_{ds} = −5 V and +5 V as a function of applied strain. (g) Energy band diagram of the p−n junction in the forward and reverse bias condition with applied mechanical strain.

depletion zone. This behavior can be explained by the piezoelectric nature of InSe.[27,28] Upon application of strain, a field develops that increases the built-in electric field of the junction. This process enhances the recombination rate of carriers from n-type and p-type channels, resulting in an increased junction conductivity.

If the strain- and light-induced barrier lowering is sufficiently high, injection through the junction area proceeds more and more efficiently compared to injection at the junction edge, as seen in a progressively increasing AAT peak current (Figure 5a). Upon application of 1.65% strain, we observe two distinct

transconductance peaks with similar PVR and narrow peak widths (Figure 5b). The bi-AAT behavior was confirmed in several InSe/WSe₂ heterojunctions under the application of strain and light illumination, as shown in Figure S10. The achievable PVR for both peaks is approximately $10^2 - 10^3$ (Figure S10d), which is comparable to previously reported AAT devices.[20,25] The transfer characteristics were observed for both forward and backward sweeping directions (Figure S11), and the device is stable for nearly 5 months when stored in vacuum conditions (Figure S12). The observed bi-AAT behavior enables advanced multilevel logic devices when
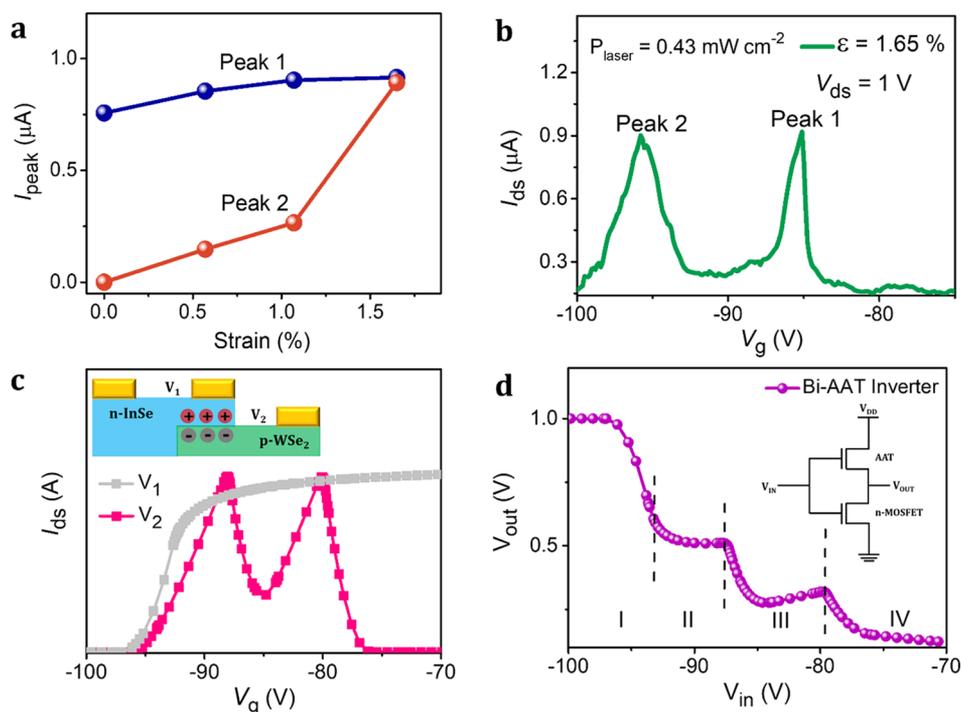
Figure 5. (a) Change in peak current (I_{peak}) as a function of strain. (b) Transfer curve at the maximum applied strain exhibiting a bi-anti-ambipolar transistor (Bi-AAT). (c) Simulated transfer curves of bi-AAT and a matched n-type MOSFET. (d) Bi-AAT as a quaternary inverter with the indication of four distinct logic levels.

integrating them with a second n-type transistor (Figure 5c), resulting in an inverter (see Supplementary Note 12). We demonstrate that in this configuration four distinct output levels are produced when varying the input voltage (Figure 5d). This quaternary (QNOT) logic gate could be integrated into a single solid-state device (see Supplementary Note 13) and thus increases the integration density of complex multilevel logic[7,34] for future electronics.

CONCLUSION

In conclusion, we have demonstrated a bi-anti-ambipolar device that exhibits two distinct transconductance peaks. Strain-dependent measurements reveal the coexistence of two conduction pathways through a 2D material heterojunction device. At low junction conductance, edge injection dominates the carrier transport, whereas high junction conductance favors injection through the junction area. Through dynamical adjustment of the two contributions, two AAT peaks with similar peak currents and peak-voltage ratios could be realized that correspond to both conduction pathways. Inverters composed of bi-AATs achieving quaternary logic in a single solid-state device can establish complex logic circuits with enhanced integration density. Thus, our proposed bi-AAT concept demonstrated in a performance-matched InSe/WSe$_2$ heterojunction can be extended to other 2D heterostructure hyperscaled electronic devices.

METHODS

Device Fabrication. InSe/WSe$_2$ heterostructures were fabricated following a dry transfer technique. First, the InSe crystal was mechanically exfoliated (Scotch tape) into few-layered flakes and transferred to the PET substrate by using a PDMS stamp. Following the same technique, the WSe$_2$ flake was also stamped exactly on top of the InSe flake on a PET substrate with the aid of a custom-made three-axis micromanipulator equipped with an optical microscope

(Olympus, BX 51M) and a CCD camera (Leica DFC495). Similarly, the exfoliated h-BN layer (Polartherm, Momentive) was also placed exactly above the InSe/WSe$_2$ heterojunction. The thickness of the as-fabricated structures was measured by AFM topography. The electrodes were patterned using a micron mesh-sized Cu grid serving as the shadow mask, and Cr/Au (7/70 nm) were deposited using a thermal evaporator.

Characterization Details. The micro-Raman spectrometer (Triax 550) furnished with an Olympus CX41 optical microscope and a Jobin Won Horiba S Drive-500 Syncernity detector was used to record the Raman and PL spectrum of the InSe/WSe$_2$ heterojunction with 2.33 eV excitation energy. A Nanosurf Flex AFM (Easyscan 2 V.3.1) was used for determining the flake thickness. A semiconductor parameter analyzer (Agilent 4156C) and a Keithley 2400 electrometer were employed to carry out the electrical measurements. For the photoresponse measurement, a 633 nm wavelength He−Ne laser was illuminated.

ASSOCIATED CONTENT

Ⓢ Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.1c00762.

> Crystal growth; crystal structure; dry transfer technique; atomic force microscopy; transistor performance; carrier transport simulation; strain calculation; photoluminescence study; device performance; carrier transport mechanism; transfer characteristics of additional Bi-AATs; quaternary inverter; improvement in device performance (PDF)

AUTHOR INFORMATION

Corresponding Authors

Mario Hofmann − *Department of Physics, National Taiwan University, Taipei 10617, Taiwan;* ⓞ orcid.org/0000-0003-1946-2478; Email: mario@phys.ntu.edu.tw

Yang-Fang Chen − *Department of Physics and Advanced Research Centre for Green Materials Science and Technology, National Taiwan University, Taipei 10617, Taiwan;* ● orcid.org/0000-0003-1203-5115; Email: yfchen@phys.ntu.edu.tw

Authors

Christy Roshini Paul Inbaraj − *Department of Engineering and System Science, National Tsing Hua University, Hsinchu 30013, Taiwan; Nano-science and Technology Program, Taiwan International Graduate Program, Academia Sinica, Taipei 11529, Taiwan; Department of Physics, National Taiwan University, Taipei 10617, Taiwan;* ● orcid.org/0000-0002-8776-9917

Roshan Jesus Mathew − *Department of Engineering and System Science, National Tsing Hua University, Hsinchu 30013, Taiwan; Nano-science and Technology Program, Taiwan International Graduate Program, Academia Sinica, Taipei 11529, Taiwan; Institute of Atomic and Molecular Sciences, Academia Sinica, Taipei 10617, Taiwan;* ● orcid.org/0000-0002-0913-6321

Rajesh Kumar Ulaganathan − *Center for Condensed Matter Sciences, National Taiwan University, Taipei 10617, Taiwan;* ● orcid.org/0000-0001-8886-6332

Raman Sankar − *Center for Condensed Matter Sciences, National Taiwan University, Taipei 10617, Taiwan; Institute of Physics, Academia Sinica, Taipei 11529, Taiwan;* ● orcid.org/0000-0003-4702-2517

Monika Kataria − *Department of Physics, National Taiwan University, Taipei 10617, Taiwan; Institute of Atomic and Molecular Sciences, Academia Sinica, Taipei 10617, Taiwan;* ● orcid.org/0000-0003-4912-340X

Hsia Yu Lin − *Department of Physics, National Taiwan University, Taipei 10617, Taiwan;* ● orcid.org/0000-0002-0886-3367

Yit-Tsong Chen − *Institute of Atomic and Molecular Sciences, Academia Sinica, Taipei 10617, Taiwan; Department of Chemistry, National Taiwan University, Taipei 10617, Taiwan;* ● orcid.org/0000-0002-6204-8320

Chih-Hao Lee − *Department of Engineering and System Science, National Tsing Hua University, Hsinchu 30013, Taiwan;* ● orcid.org/0000-0002-3898-6421

Complete contact information is available at:
https://pubs.acs.org/10.1021/acsnano.1c00762

Notes

The authors declare no competing financial interest.

REFERENCES

(1) Kobashi, K.; Hayakawa, R.; Chikyow, T.; Wakayama, Y. Multi-Valued Logic Circuits Based on Organic Anti-Ambipolar Transistors. *Nano Lett.* **2018**, *18*, 4355−4359.

(2) Smith. The Prospects for Multivalued Logic: A Technology and Applications View. *IEEE Trans. Comput.* **1981**, *3*, 619−634.

(3) Waho, T.; Chen, K. J.; Yamamoto, M. Resonant-Tunneling Diode and HEMT Logic Circuits with Multiple Thresholds and Multilevel Output. *IEEE J. Solid-State Circuits* **1998**, *33*, 268−274.

(4) Shim, J.; Oh, S.; Kang, D. H.; Jo, S. H.; Ali, M. H.; Choi, W. Y.; Heo, K.; Jeon, J.; Lee, S.; Kim, M.; Song, Y. J.; Park, J. H. Phosphorene/Rhenium Disulfide Heterojunction-Based Negative Differential Resistance Device for Multi-Valued Logic. *Nat. Commun.* **2016**, *7*, 13413.

(5) Kobashi, K.; Hayakawa, R.; Chikyow, T.; Wakayama, Y. Interface Engineering for Controlling Device Properties of Organic Anti-ambipolar Transistors. *ACS Appl. Mater. Interfaces* **2018**, *10*, 2762−2767.

(6) Shim, J.; Jo, S. H.; Kim, M.; Song, Y. J.; Kim, J.; Park, J. H. Light-Triggered Ternary Device and Inverter Based on Heterojunction of van der Waals Materials. *ACS Nano* **2017**, *11*, 6319−6327.

(7) Lim, J. H.; Shim, J.; Kang, B. S.; Shin, G.; Kim, H.; Andreev, M.; Jung, K. S.; Kim, K. H.; Choi, J. W.; Lee, Y.; Park, J. H. Double Negative Differential Transconductance Characteristic: From Device to Circuit Application toward Quaternary Inverter. *Adv. Funct. Mater.* **2019**, *29*, 1905540.

(8) Mudd, G. W.; Svatek, S. A.; Ren, T.; Patanè, A.; Makarovsky, O.; Eaves, L.; Beton, P. H.; Kovalyuk, Z. D.; Lashkarev, G. V.; Kudrynskyi, Z. R.; Dmitriev, A. I. Tuning the Bandgap of Exfoliated InSe Nanosheets by Quantum Confinement. *Adv. Mater.* **2013**, *25*, 5714−5718.

(9) Yeh, P. C.; Jin, W.; Zaki, N.; Zhang, D.; Liou, J. T.; Sadowski, J. T.; Al-Mahboob, A.; Dadap, J. I.; Herman, I. P.; Sutter, P.; Osgood, R. M. Layer-Dependent Electronic Structure of an Atomically Heavy Two-Dimensional Dichalcogenide. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2015**, *91*, 041407.

(10) Zhao, W.; Ghorannevis, Z.; Chu, L.; Toh, M.; Kloc, C.; Tan, P. H.; Eda, G. Evolution of Electronic Structure in Atomically Thin Sheets of WS$_2$ and WSe$_2$. *ACS Nano* **2013**, *7*, 791−797.

(11) Sucharitakul, S.; Goble, N. J.; Kumar, U. R.; Sankar, R.; Bogorad, Z. A.; Chou, F. C.; Chen, Y. T.; Gao, X. P. A. Intrinsic Electron Mobility Exceeding $10^3 cm^2/(V\ s)$ in Multilayer InSe FETs. *Nano Lett.* **2015**, *15*, 3815−3819.

(12) Zhou, H.; Wang, C.; Shaw, J. C.; Cheng, R.; Chen, Y.; Huang, X.; Liu, Y.; Weiss, N. O.; Lin, Z.; Huang, Y.; Duan, X. Large Area Growth and Electrical Properties of *p*-Type WSe$_2$ Atomic Layers. *Nano Lett.* **2015**, *15*, 709−713.

(13) Di Bartolomeo, A.; Urban, F.; Passacantando, M.; McEvoy, N.; Peters, L.; Iemmo, L.; Luongo, G.; Romeo, F.; Giubileo, F. A WSe$_2$ Vertical Field Emission Transistor. *Nanoscale* **2019**, *11*, 1538−1548.

(14) Liu, Y.; Weiss, N. O.; Duan, X.; Cheng, H. C.; Huang, Y.; Duan, X. van der Waals Heterostructures and Devices. *Nat. Rev. Mater.* **2016**, *1*, 16042.

(15) Paul Inbaraj, C. R.; Mathew, R. J.; Ulaganathan, R. K.; Sankar, R.; Kataria, M.; Lin, H. Y.; Cheng, H. Y.; Lin, K. H.; Lin, H. I.; Liao, Y. M.; Chou, F. C.; Chen, Y. T.; Lee, C. H.; Chen, Y. F. Modulating Charge Separation with Hexagonal Boron Nitride Mediation in Vertical van der Waals Heterostructures. *ACS Appl. Mater. Interfaces* **2020**, *12*, 26213−26221.

(16) Carlone, C.; Jandl, S.; Shanks, H. R. Optical Phonons and Crystalline Symmetry of InSe. *Phys. Status Solidi B* **1981**, *103*, 123−130.

(17) Tonndorf, P.; Schmidt, R.; Böttger, P.; Zhang, X.; Börner, J.; Liebig, A.; Albrecht, M.; Kloc, C.; Gordan, O.; Zahn, D. R. T.; Michaelis de Vasconcellos, S.; Bratschitsch, R. Photoluminescence Emission and Raman Response of Monolayer MoS$_2$, MoSe$_2$, and WSe$_2$. *Opt. Express* **2013**, *21*, 4908−4916.

(18) Park, C. J.; Park, H. J.; Lee, J. Y.; Kim, J.; Lee, C. H.; Joo, J. Photovoltaic Field-Effect Transistors Using a MoS$_2$ and Organic

Rubrene van der Waals Hybrid. *ACS Appl. Mater. Interfaces* **2018**, *10*, 29848−29856.

(19) Dong, J.; Liu, F.; Wang, F.; Wang, J.; Li, M.; Wen, Y.; Wang, L.; Wang, G.; He, J.; Jiang, C. Configuration-Dependent Anti-Ambipolar van der Waals *p-n* Heterostructures Based on Pentacene Single Crystal and MoS_2. *Nanoscale* **2017**, *9*, 7519−7525.

(20) Li, Y.; Wang, Y.; Huang, L.; Wang, X.; Li, X.; Deng, H. X.; Wei, Z.; Li, J. Anti-Ambipolar Field-Effect Transistors Based on Few-Layer 2D Transition Metal Dichalcogenides. *ACS Appl. Mater. Interfaces* **2016**, *8*, 15574−15581.

(21) Nourbakhsh, A.; Zubair, A.; Dresselhaus, M. S.; Palacios, T. Transport Properties of a MoS_2/WSe_2 Heterojunction Transistor and Its Potential for Application. *Nano Lett.* **2016**, *16*, 1359−1366.

(22) Yao, H.; Hsieh, Y. P.; Kong, J.; Hofmann, M. Modelling Electrical Conduction in Nanostructure Assemblies through Complex Networks. *Nat. Mater.* **2020**, *19*, 745−751.

(23) Kobashi, K.; Hayakawa, R.; Chikyow, T.; Wakayama, Y. Device Geometry Engineering for Controlling Organic Antiambipolar Transistor Properties. *J. Phys. Chem. C* **2018**, *122*, 6943−6946.

(24) Paul, A. K.; Kuiri, M.; Saha, D.; Chakraborty, B.; Mahapatra, S.; Sood, A. K.; Das, A. Photo -Tunable Transfer Characteristics in $MoTe_2$-MoS_2 Vertical Heterostructure. *npj 2D Mater. Appl.* **2017**, *1*, 17.

(25) Wang, Y.; Zhou, W. X.; Huang, L.; Xia, C.; Tang, L. M.; Deng, H. X.; Li, Y.; Chen, K. Q.; Li, J.; Wei, Z. Light-Induced Double "On" State Anti-Ambipolar Behavior and Self-Driven Photoswitching in *p*-WSe_2/*n*-SnS_2 Heterostructures. *2D Mater.* **2017**, *4*, 025097.

(26) Wakayama, Y.; Hayakawa, R. Antiambipolar Transistor: A Newcomer for Future Flexible Electronics. *Adv. Funct. Mater.* **2020**, *30*, 1903724.

(27) Li, Y.; Wang, T.; Wu, M.; Cao, T.; Chen, Y.; Sankar, R.; Ulaganathan, R. K.; Chou, F.; Wetzel, C.; Xu, C. Y.; Louie, S. G.; Shi, S. F. Ultrasensitive Tunability of the Direct Bandgap of 2D InSe Flakes *via* Strain Engineering. *2D Mater.* **2018**, *5*, 021002.

(28) Paul Inbaraj, C. R.; Mathew, R. J.; Haider, G.; Chen, T. P.; Ulaganathan, R. K.; Sankar, R.; Bera, K. P.; Liao, Y. M.; Kataria, M.; Lin, H. I.; Chou, F. C.; Chen, Y. T.; Lee, C. H.; Chen, Y. F. Ultra-High Performance Flexible Piezopotential Gated $In_{1-x}Sn_xSe$ Photo-transistor. *Nanoscale* **2018**, *10*, 18642−18650.

(29) Dhakal, K. P.; Roy, S.; Jang, H.; Chen, X.; Yun, W. S.; Kim, H.; Lee, J.; Kim, J.; Ahn, J. H. Local Strain Induced Band Gap Modulation and Photoluminescence Enhancement of Multilayer Transition Metal Dichalcogenides. *Chem. Mater.* **2017**, *29*, 5124−5133.

(30) Desai, S. B.; Seol, G.; Kang, J. S.; Fang, H.; Battaglia, C.; Kapadia, R.; Ager, J. W.; Guo, J.; Javey, A. Strain-Induced Indirect to Direct Bandgap Transition in Multilayer WSe_2. *Nano Lett.* **2014**, *14*, 4592−4597.

(31) Zhao, W.; Ribeiro, R. M.; Toh, M.; Carvalho, A.; Kloc, C.; Castro Neto, A. H.; Eda, G. Origin of Indirect Optical Transitions in Few-Layer MoS_2, WS_2, and WSe_2. *Nano Lett.* **2013**, *13*, 5627−5634.

(32) Lukman, S.; Ding, L.; Xu, L.; Tao, Y.; Riis-Jensen, A. C.; Zhang, G.; Wu, Q. Y. S.; Yang, M.; Luo, S.; Hsu, C.; Yao, L.; Liang, G.; Lin, H.; Zhang, Y. W.; Thygesen, K. S.; Wang, Q. J.; Feng, Y.; Teng, J. High Oscillator Strength Interlayer Excitons in Two-Dimensional Heterostructures for Mid-Infrared Photodetection. *Nat. Nanotechnol.* **2020**, *15*, 675−682.

(33) Paul Inbaraj, C. R.; Gudelli, V. K.; Mathew, R. J.; Ulaganathan, R. K.; Sankar, R.; Lin, H. Y.; Lin, H.-I.; Liao, Y.-M.; Cheng, H.-Y.; Lin, K.-H.; Chou, F. C.; Chen, Y.-T.; Lee, C.-H.; Guo, G.-Y.; Chen, Y.-F. Sn-Doping Enhanced Ultrahigh Mobility $In_{1-x}Sn_xSe$ Phototransistor. *ACS Appl. Mater. Interfaces* **2019**, *11*, 24269−24278.

(34) Han, H.; Kim, C. H. Prediction of a Two-Transistor Vertical QNOT Gate. *Appl. Sci.* **2020**, *10*, 7597.